Cunxi Yu **last update: 04/2022**

Contact Information

University of Utah
Office: 2126 MEB, ECE Department
Address: 2126 MEB, 50 S Central Campus Dr #2110, Salt Lake City, UT 84112
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Web: https://ycunxi.github.io/cunxiyu/

Research Interests

Formal Methods, Design Automation, Emerging Computing and Acceleration, System and Compiler, Security, Applied Machine Learning

Research Appointments

University of Utah, Salt Lake City, Utah, USA
Assistant Professor **08.2019 - present**

Cornell University, Ithaca, NY, USA
Post-Doc **09.2018 - 07.2019**
Advisor: Prof. Zhiru Zhang
Research focus: Machine learning for Hardware Design Automation

Swiss Federal Institute of Technology in Lausanne (EPFL), Lausanne, Switzerland
Post-Doc **08.2017 - 08.2018**
Advisor: Prof. Giovanni De Micheli
Research focus: Machine learning for Hardware Design Automation

University of Massachusetts Amherst, Amherst, MA, USA
Research Assistant **01.2014 - 07.2017**
Advisor: Prof. Maciej Ciesielski
Research focus: Formal Methods, Hardware Security

IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA
Research Intern, Design Automation Research **05.2016 - 11.2016**
Research Intern, Design Automation Research **05.2015 - 09.2015**
Research focus: Hardware acceleration, EDA

Education

University of Massachusetts Amherst, Massachusetts, USA

Ph.D. Computer Engineering **05.2017**

- Dissertation: "Formal Analysis of Arithmetic Circuits using Computer Algebra - Verification, Abstraction and Reverse Engineering."

Zhejiang University City College, Hangzhou, China

B.S. Electrical Engineering **06.2013**

Awards

- NSF CAREER Award (2021)
- 2017 ASP-DAC Best Paper Nomination
- ACM Doctoral Dissertation Award Nomination (by UMass Amherst)
- DAC 2017 Security Contest - 1st Place
- 2017 IWLS Student Grant
- 2016 IEEE TVLSI Travel Grant
- IEEE TCAD Best Paper Nomination (2016)

Publications

Author keys: * Equal contributions; __ Students advised; † Communication author.

2022

- Ecenur Ustun, Ismail San, Jiaqi Yin, **Cunxi Yu**, and Zhiru Zhang. *Exact Memory- and Communication-Aware Scheduling of DNNs on Pipelined Edge TPUs.* IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM'22).
- Jiaqi Yin, Zhiru Zhang, **Cunxi Yu**. *IMpress: Large Integer Multiplication Expression Rewriting for FPGA HLS* ACM/IEEE International Symposium on Edge Computing (SEC'22) (16.7%,to appear).
- Yingheng Tang, Jichao Fan, Xinwei Li, Jianzhu Ma, Minghao Qi, **Cunxi Yu**†, Weilu Gao†. *Physics-Guided and Physics-Explainable Recurrent Neural Network for Time Dynamics in Optical Resonances. Nature Computational Science.* 2.3 (2022): 169-178.
- Yingjie Li, Weilu Gao, **Cunxi Yu**. *Rubik's Optical Neural Networks: Multi-task Learning with Physics-aware Training. Design Automation Conference (DAC'22) WIP.*
- Jiaqi Yin, Qiwei Yuan, Yingjie Li, **Cunxi Yu**. *Combinatorial Reinforcement Learning Based Scheduling for DNN Execution on Edge. TinyML Research Symposium 2022* (TinyML'22).

2021

- Yingjie Li, Minhan Lou, Ruiyang Chen, Jichao Fan, Berardi Sensale Rodriguez, Weilu Gao, **Cunxi Yu**. *LightRidge: End-to-end Photonic Compiler Framework for Diffractive Optical Neural Networks.* ROAD4NN Workshop at 58th Design Automation Conference (DAC'21).
- Yingjie Li, **Cunxi Yu**. *LBR: Physical Adversarial Attacks of Diffractive Deep Neural Networks. 58th Design Automation Conference* (DAC'21).
- Yingjie Li, Ruiyang Chen, Berardi Sensale Rodriguez, Weilu Gao, **Cunxi Yu**. *Multi-Task Learning in Diffractive Deep Neural Networks via Hardware-Software Co-design. Nature Scientific Reports.* 2021.
- Walter Lau Neto, Matheus Trevisan Moreira, Yingjie Li, Luca Amaru, **Cunxi Yu**, and Pierre-Emmanuel Gaillardon *SLAP: A Supervised Learning Approach for Priority Cuts Technology Mapping. 58th Design Automation Conference* (DAC'21).
- Weilu Gao, **Cunxi Yu**, Ruiyang Chen. *Artificial Intelligence Accelerators based on Graphene Optoelectronic Devices. Advanced Photonics Research.*
- Walter Lau Neto, Matheus Trevisan Moreira, Luca Amaru, **Cunxi Yu**, and Pierre-Emmanuel Gaillardon. *Read your Circuit: Leveraging Word Embedding to Guide Logic Optimization. ASPDAC'21.*

2020

- **Cunxi Yu**. *FlowTune: Practical Multi-Arm Bandits in Boolean Optimization.* ICCAD'2020.
- **Cunxi Yu**, Wang Zhou. *Decision Making in Synthesis cross Technologies using LSTMs and Transfer Learning. MLCAD'2020.*
- Walter Lau Neto, Matheus Trevisan Moreira, Luca Amaru, **Cunxi Yu**, and Pierre-Emmanuel Gaillardon. *EaSyOpt: Predicting Post Place and Route Critical Paths for Early Synthesis Optimization* (IWLS'2020).

2019

- **Cunxi Yu**, Zhiru Zhang. *Painting on Placement: Forecasting Routing Congestion using Conditional Generative Adversarial Nets.* ACM/IEEE Design Automation Conference (DAC'19)
- **Cunxi Yu**, Atif Yasin, Tiankai Su and Maciej Ciesielski. *Spectral Approach to Verifying Nonlinear Arithmetic Circuits.* ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC'19)

- Maciej Ciesielski, Atif Yasin, Tiankai Su, **Cunxi Yu**. *Understanding Algebraic Rewriting for Arithmetic Circuit Verification: a Bit-Flow Model.* (TCAD'19)
- Ecenur Ustun, Shaojie Xiang, Jinny Gui, **Cunxi Yu**, Zhiru Zhang. *LAMDA: Learning-Assisted Multi-stage Design Autotuning.* IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'19)

2018

- **Cunxi Yu**, Atif Yasin, Tiankai Su, Alan Mishchenko and Maciej Ciesielski. *Rewriting Environment for Arithmetic Circuit Verification.* International Conference on Logic for Programming Artificial Intelligence and Reasoning (LPAR-22), Nov 2018.
- **Cunxi Yu**, Houping Xiao, Giovanni De Micheli. *Developing Synthesis Flows without Human Knowledge.* ACM/IEEE Design Automation Conference (DAC'18)
- **Cunxi Yu**, Maciej Ciesielski and Alan Mishchenko. *Fast Computer Algebra Rewriting based on And-Inv-Graphs.* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).
- **Cunxi Yu** and Maciej Ciesielski. *Formal Analysis of Galois Field Arithmetic -Verification and Reverse Engineering in Parallel.* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).
- **Cunxi Yu**, Heinz Riener, Francesca Stradolini, Giovanni De Micheli. *Generating Safety Guidance for Medical Injection with Three-Compartment Pharmacokinetics Model.* (ISVLSI'18)
- **Cunxi Yu**, Gi-Joon Nam, Mihir Choudhury, Victor Kravets, Andrew Sullivan and Maciej Ciesielski, Giovanni De Micheli. *End-to-End Industrial Study of Retiming.* (ISVLSI'18).
- Shahrzad Keshavarz, **Cunxi Yu**, Samaneh Ghandali, Xiaolin Xu, Daniel Holcomb. *Survey on applications of formal methods in reverse engineering and intellectual property protection.* (**Invited**) Journal of Hardware and Systems Security - Springer.
- Tiankai Su, **Cunxi Yu**, Atif Yasin, Maciej Ciesielski. *Computer Algebraic Approach for Galois Field Multipliers Verification and Debugging.* 2018 IEEE International Symposium on Circuits and Systems (ISCAS'18)

2017

- **Cunxi Yu**, Mihir Choudhury, Andrew Sullivan and Maciej Ciesielski. *Advanced Datapath Synthesis using Graph Isomorphism.* 2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD'17), Irvine, CA, USA, November 13-16, 2017.
- **Cunxi Yu** , Daniel Holcomb and Maciej Ciesielski. *Reverse Engineering Irreducible Polynomial of GF(*2^m*) Arithmetic.* Design Automation and Test in Europe (DATE'17). March, 2017. Lausanne, Switzerland.
- **Cunxi Yu** and Maciej Ciesielski. *Efficient Parallel Verification of Galois Field Multipliers.* Asia and South Pacific Design Automation Conference (ASP-DAC'17). pp. 238 - 243. January, 2017. Chia/Tokyo, Japan. (**Best Paper Award Nomination**).
- **Cunxi Yu**, Xiangyu Zhang, Duo Liu, Maciej Ciesielski, Daniel Holcomb. *Incremental SAT-based Reverse Engineering of Camouflaged Logic Circuits.* 2017 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).
- Tiankai Su, **Cunxi Yu**, Atif Yasin, Maciej Ciesielski. *Formal Verification of Truncated Multipliers using Algebraic Approach and Re-synthesis.* 2017 IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2017, Bochum, Germany, July 3-5, 2017.

2016

- **Cunxi Yu**, Walter Brown, Duo Liu, Andre Rossi and Maciej Ciesielski. *Formal Verification of Arithmetic Circuits by Function Extraction.* IEEE Trans. on CAD of Integrated Circuits and Systems (TCAD'16) 35(12): 2131-2142 (2016). (**Best Paper Nomination**)
- **Cunxi Yu** and Maciej Ciesielski. *Formal Verification using Don't-care and Vanishing Polynomials.* 2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI'16) , July 2016, Pittsburgh USA.
- **Cunxi Yu** and Maciej Ciesielski. *Analyzing Imprecise Adders using BDDs - A Case Study.* 2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI'16) , July 2016, Pittsburgh, USA.
- **Cunxi Yu**, Mihir Choudhury, Andrew Sullivan and Maciej Ciesielski. *DAG-Aware Logic synthesis of Datapaths.* 53rd Design Automation Conference (DAC'16), June 2016, Austin, USA.
- **Cunxi Yu**, Maciej Ciesielski. *Automatic Word-level Abstraction on Datapaths.* IEEE International Symposium on Circuits and System (ISCAS'16), May 2016, Montreal, Canada.
- Duo Liu, **Cunxi Yu**, Xiangyu Zhang, Daniel Holcomb. *Oracle-Guided Incremental SAT Solving to Reverse Engineer Camouflaged Logic Circuits.* Design, Automation and Test in Europe (DATE'16) March 2016, Dresden, Germany.

2015

- **Cunxi Yu**, Duo Liu, Walter Brown, Samaneh Ghandali, Maciej Ciesielski. Verification of Sequential Arithmetic Circuit. 52nd Design Automation Conference, June 2015, San Fransisco, CA, USA. (*DAC'15-WIP*).
- **Cunxi Yu**, Walter. Brown, Maciej. Ciesielski. *Verification of Arithmetic Datapath Designs using Word-level Approach.* 2015 IEEE International Symposium on Circuits and System (ISCAS'15) IEEE, May 2015, Lisbon, Portugal .
- Samaneh Ghandali, **Cunxi Yu**, Duo Liu, Maciej Ciesielski. *Logic Debugging of Arithmetic Circuits.* 2015 IEEE Computer Society Annual Symposium on VLSI (ISVLSI'15) , July 2016, Montpellier, France.
- Maciej Ciesielski, **Cunxi Yu**, Walter Brown, Duo Liu, Andre Rossi. *Verification of Gate-level Arithmetic Circuits by Function Extraction.* 52nd Design Automation Conference (DAC'15), June 2015, San Francisco, USA.
- Samaneh Ghandali, **Cunxi Yu**, Duo Liu, Maciej Ciesielski. Diagnosis and Debugging of Arithmetic Circuits. 52nd Design Automation Conference, June 2015, San Fransisco, CA, USA. (*DAC'15-WIP*).

Grants

On-going

- *NSF: CAREER: CAREER: OneSense: One-Rule-for-All Combinatorial Boolean Synthesis via Reinforcement Learning.* NSF-#2008144, 09.01.2021 - 08.31.2026. Amount: $478,526.00
  PI: Cunxi Yu, University of Utah.
- *NSF: SHF: Small: Boosting Boolean Reasoning with Inductive Attributed Graph Learning.* NSF-#2008144, 09.01.2020 - 08.31.2023. Amount: $381,707.00.
  PI: Cunxi Yu, University of Utah.
- *NSF: FMiTF: Collaborative: DeepSmith: Scheduling with Quality Guarantees for Efficient DNN Model Execution.* NSF-#2019336, 09.01.2020 - 08.31.2024. Amount: $743,000.00.
  PI: Cunxi Yu (50%), University of Utah; co-PI: Zhiru Zhang (50%), Cornell University.
- *NSF: I-Corps: Heterogeneous HPC Compiler Framework for Hardware-Software Optical AI Accelerator Co-Design.* 2021. Amount: $6,000.
  PI: Weilu Gao (50%), **co-PI: Cunxi Yu** (50%). University of Utah.

Open-source Tools

LightRidge: Compiler Framework for Optical Neural Networks
https://lightridge.github.io/lightridge/

Intelligent Hardware Synthesis Systems [ICCAD'2020,DAC'18]
FlowTune: https://github.com/Yu-Utah/FlowTune
FlowGen: https://github.com/ycunxi/FLowGen-CNNs-DAC18

ACEC: **A**rithmetic **C**ombinational **E**quivalence **C**hecking [Ph.D. Thesis][DAC'15] [TCAD'17,'19]
https://github.com/ycunxi/abc
https://github.com/ycunxi/Parallel_Formal_Analysis_GaloisField

Incremental-SAT De-camouflaging for Encrypted Logic Circuits [DATE'16] [TCAD'16]
https://github.com/ycunxi/Incremental-SAT-DeCam

Teaching Experience

University of Utah

- Instructor. ECE/CS 5740/6740 - CAD of Digital Circuits. University of Utah. Spring'21, Spring'22
- Instructor. ECE/CS 3700 - Digital System Design. University of Utah. Fall'20, Fall'21, Fall'22
- Instructor. ECE 5960/6960 - Deep Learning Systems. University of Utah. Spring'20, Spring'22

Before joining University of Utah

- Teaching Assistant. ECE 667 - Synthesis and Verification. UMass Amherst. Spring 2016 (Graduate level)
- Teaching Assistant. ECE 221 - Introduction to Digital Systems. UMass Amherst. Fall 2015.
- Teaching Assistant. ECE 597/697 MB - Embedded Systems. Spring 2015. (Graduate level)

Services

Organizing Committee: ASAP'19, IWLS'20–22, VLSI-SoC'20, ICCD'20–21

TPC Member: IWLS'17-20, DUHDe@DATE'19, ASPDAC'20, ICCAD'20, ASPDAC'21, ICCAD'21, DAC'22, ICCAD'22

Reviewer: VTS'15, ICCAD'15, CHES'16, DAC'17, DATE'18, DAC'18, ASP-DAC'19, FPGA'19

Journal Editor:
Journal of Signal Processing Systems (Guest Editor)

Journal Reviewer:
ACM Transactions on Design Automation of Electronic Systems
IEEE Design & Test of Computers
IEEE Transactions on Very Large Scale Integration Systems
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
IEEE Transactions on Computers
IEEE Transactions on Information Forensics and Security
IEEE Journal on Emerging and Selected Topics in Circuits and Systems
IEEE Transactions on Emerging Topics in Computing

Mentoring Experience

University of Utah

- Yingjie Li, Ph.D. student (Chair).
- Jiaqi Yin, Ph.D. student (Chair).
- Tara Zamani, M.S. thesis (Chair).
- Walter Lau, Ph.D. student (Committee) *Advanced Logic Synthesis System.*
- Aurelien Alacchi, Ph.D. student (Committee) *Smart FPGA Architecture for Reliability Improvement in Harsh Environments.*
- Max Austin, Ph.D. student (Committee) *Integration of Machine Learning in Logic Synthesis..*
- Venkata Sai MadhuKiran Harsha Nori, Ph.D. student (Committee) *Scalable Asynchronous Circuit Design.*
- Ziyi Chen, Ph.D. student (Committee) *Non-Convex Optimization Theories and Applications.*

Cornell University

- Shaojie Xiang, Ph.D. student. *EZTune: A Generic Auto-tuning Language and Framework.*
- Zhijing Li and Chenhui Deng, Ph.D. student. *HLS Performance Estimation using Graph Learning.*
- Ecenur Ustun (Ph.D.), Jinny Gui (B.S.). *Learning Assisted Design Closure System for FPGAs.*

UMass Amherst

- Tiankai Su,Ph.D. student. *Formal Verification of Approximate Arithmetic Circuits* [ISCAS'18, ASP-DAC'19]
- Atif Yasin, Ph.D. student. *Logic Diagnosis based on Gröbner basis.* [ISCAS'18, ASP-DAC'19]
- Walter Brown, *Honor* B.S project. *Logic Debugging using Machine Learning.*
- Michael Shliselberg and Jordan Kaplan. *NSF-REU*, Summer 2015. *Formal Verification and Logic Synthesis of Arithmetic Circuits.*